Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

35.   A memory device comprising:

a plurality of memory cells, each of which is readable by application of a read voltage; and

means for determining a likelihood that the memory device has a degraded state by applying each of a plurality of read voltages to a terminal of a first cell of the plurality of memory cells to generate a plurality of read results.

36.(Previously Amended) The memory device of claim 35, wherein a group of the plurality of memory cells are arranged in a row that includes the first cell, the memory device further comprising means for rewriting a previously stored value into each of the group of memory cells when the means for determining determines that the first cell has a degraded state.

(Claim 37 has been cancelled.)

38.   The memory device of claim 35, wherein:

a group of the plurality of memory cells are arranged in a row that includes the first cell; and

the means for determining includes means for determining the likelihood by applying each of the plurality of read voltages when a write is performed on the group of memory cells.

39.   The memory device of claim 35, wherein:

a group of the plurality of memory cells are arranged in a row that includes the first cell; and

the means for determining includes means for determining the likelihood by applying each of the plurality of read voltages when a read is performed on the group of memory cells.

40.   The memory device of claim 35, wherein the terminal of the first cell is a control gate terminal of the first cell.

(Claims 41-44 have been cancelled.)

45.(Previously Amended)   A method of operating a memory device having a plurality of memory cells, comprising:

generating a first read voltage;

applying said first read voltage to a terminal of a first cell of the plurality of memory cells;

generating a first read result in response to said applying said first read voltage;

generating a second read voltage;

applying said second read voltage to said terminal of said first cell;

generating a second read result in response to said applying said second read voltage; and

determining from said first and second read results whether data storage of the memory device is deteriorated.

(Claims 46 and 47 have been cancelled.)

48.   The method of claim 45, wherein said method is part of a programming process.

49.   The method of claim 45, wherein said method is part of a reading process.

50.   The method of claim 45, wherein said memory cells are multi-state memory cells.

51.   The method of claim 45, wherein said memory cells are floating gate transistors and said terminal is a control gate.